

	L #	Hits	Search Text	DBs	Time Stamp
1	L1	19578	(tft or thin adj film adj transistor) and glass adj substrate	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27. 09:08
2	L2	222	dry adj etch and 1	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:09
3	L3	95	polysilicon and 2	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:09
4	L4	73	3 and ((@ad<"20020912") or (@rlad<"20020912"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:15

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	6978 4	(dry adj etch) or isotropic	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:13
6	L6	1637	undercut near4 metal	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:14
7	L7	2	5 with 6 with implant\$6	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:14
8	L8	57	implant\$6 with ions with (ldd or "lightly doped drain") with metal with mask	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:15

	L #	Hits	Search Text	DBs	Time Stamp
9	L9	42	8 and ((@ad<"20020912") or (@rlad<"20020912"))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:15
10	L10	1	("6329672").PN.	US- PGPUB; USPAT; USOCR	2005/05/27 09:30
11	L11	0	("6677189").URPN.	USPAT	2005/05/27 09:30
12	L12	2	("20020094639").PN.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:41
13	L13	335	(438/163).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:41

	L #	Hits	Search Text	DBs	Time Stamp
14	L14	700	(438/164).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:41
15	L15	1168	(438/151).CCLS.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:41
16	L16	1988	13 or 14 or 15	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:42
17	L17	4	16 and 9	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	2005/05/27 09:42

US-PAT-NO: 6677189

DOCUMENT-IDENTIFIER: US 6677189 B2

TITLE: Method for forming polysilicon thin film transistor with a self-aligned LDD structure

----- KWIC -----

Application Filing Date - AD (1):

20011130

Brief Summary Text - BSTX (11):

The method of forming the polysilicon thin film transistor with the self-aligned LDD structure comprises steps of: (a) providing a transparent insulating substrate with a polysilicon layer formed on the substrate and a gate insulating layer formed on the polysilicon layer; (b) forming a first metal layer, a second metal layer, and a patterned photoresist layer, successively, on the entire surface of the substrate; (c) dry etching to remove the second metal layer and the first metal layer not covered by the patterned photoresist layer; (d) performing a first ion implantation process with the patterned photoresist layer as a mask to form a heavily doped region on the peripheral region of the polysilicon layer; (e) wet etching to remove a part of the peripheral region of the second metal layer so as to expose a part of the peripheral region of the first metal layer; (f) removing the patterned photoresist layer; (g) dry etching to remove the exposed region of the first metal layer so as to level off the sidewalls of the second metal layer and the first metal layer.; and (h) performing a second ion implantation process with the first metal layer and the second metal layer as a mask to form a lightly doped region on the undoped region of the polysilicon layer.